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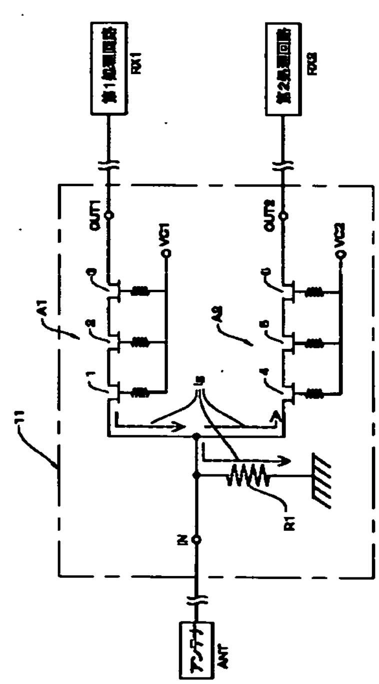
(54)【発明の名称】　ＩＣスイッチ

(57)【要約】
【課題】　従来のＩＣスイッチには以下の問題があった。共通な第１端子と第２，第３端子間の接続を、それぞれに直列接続された接合型のＦＥＴのＯＮ／ＯＦＦにより切換えるＩＣスイッチでは、ゲート電流Ｉｇが小さいためゲート電圧ＶＧとピンチオフ電圧ＶＰとの差が少なく信号（交流波形）が入力されたときＯＮ動作中のＦＥＴをＡＣ的にＯＦＦさせてしまうことがあり挿入損失が生じた。
【解決手段】　ＩＣスイッチ１１は、入力端子ＩＮと第１出力端子ＯＵＴ１間の第１伝送経路Ａ１と、入力端子ＩＮと第２出力端子ＯＵＴ２間の第２伝送経路Ａ２に、それぞれ例えば３個の接合型のＦＥＴ１～３，４～６を直列接続し、入力端子ＩＮを抵抗Ｒ１を介して接地している。この抵抗Ｒ１は入力端子ＩＮへの信号が最大時にＯＮ側のＦＥＴの制御電圧VC_{High}と入力端子ＩＮの電位の差がピンチオフ電圧ＶＰより大きくなる抵抗値に設定した抵抗Ｒ１である。



【特許請求の範囲】

【請求項１】共通の第１端子と第２端子および第３端子の間にそれぞれ接合型のＦＥＴを接続し、各ＦＥＴを交互にＯＮ，ＯＦＦ動作させ第１端子と第２端子および第３端子との間を開閉制御するＩＣスイッチにおいて、上記共通の第１端子を抵抗を介して接地し、この抵抗の抵抗値を第１端子への信号が最大時にＯＮ動作中のＦＥＴのゲート電位と第１端子の電位との電位差がＦＥＴのピンチオフ電圧より大きくなるように設定したことを特徴とするＩＣスイッチ。

【請求項２】第１端子を入力端子，第２端子および第３端子を出力端子とする１入力２出力型であることを特徴とする請求項１に記載のＩＣスイッチ。

【請求項３】前記接合型のＦＥＴはガリウムヒ素ＦＥＴであることを特徴とする請求項１に記載のＩＣスイッチ。

【請求項４】前記ＦＥＴが複数個、直列接続されたことを特徴とする請求項１に記載のＩＣスイッチ。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は共通な第１端子と第２，第３端子間の接続を接合型のＦＥＴにより切換えるＩＣスイッチに関する。

〔発明の詳細な説明〕

【０００２】

【従来の技術】移動体通信等に用いられる送受信等の高周波信号の切換用スイッチは低挿入損失及び高出力が要求され、異なる周波数の信号を切換えるためのスイッチでは広帯域特性も要求される。このようなスイッチとして携帯電話の受信切換えに用いるＩＣスイッチについて説明する。

【０００３】図３は従来の１入力２出力型のＩＣスイッチの構成を示す等価回路図であり、図４は接合型のＦＥＴのＩＤ－ＶＧ特性とＲＦ信号による入出力端子の電圧の変動との関係を示す説明図である。

【０００４】図３に示すＩＣスイッチ１０（図中の一点鎖線で囲んだ部分）は、入力端子ＩＮと第１出力端子ＯＵＴ１間の第１伝送経路Ａ１と、入力端子ＩＮと第２出力端子ＯＵＴ２間の第２伝送経路Ａ２に、それぞれ例えば３個の接合型のＦＥＴ１～３，４～６を直列に接続している。また、入力端子ＩＮ，第１出力端子ＯＵＴ１，第２出力端子ＯＵＴ２はＩＣスイッチ１０外部にあるアンテナＡＮＴ，ＲＦ信号を処理する後段の第１処理回路ＲＸ１，第２処理回路ＲＸ２にそれぞれ接続している。ＦＥＴ１～６は例えばディプレッション形のｎチャンネル形ガリウムヒ素接合型ＦＥＴであり、ゲート電圧ＶＧがピンチオフ電圧ＶＰに対してＶＰ＜ＶＧの範囲でドレインとソース間は低インピーダンスとなりＯＮになり、ＶＧ＜ＶＰの範囲でドレインとソース間は高インピーダンスとなりＯＦＦになる。ここで複数のＦＥＴを直列接続しているのはＲＦ信号に対する耐電力性を向上させるためである。

【０００５】次に、ＩＣスイッチ１０の機能と動作について説明する。ＦＥＴ１～３は第１制御電圧ＶＣ１でＯＮ／ＯＦＦ制御され、また、ＦＥＴ４～６は第２制御電圧ＶＣ２でＯＮ／ＯＦＦ制御される。第１制御電圧ＶＣ１と第２制御電圧ＶＣ２とは相補的に印加され、ＦＥＴ１～３がＯＮのときＦＥＴ４～６はＯＦＦとなり、ＦＥＴ１～３がＯＦＦのときＦＥＴ４～６はＯＮとなり第１伝送経路Ａ１または第２伝送経路Ａ２のいずれか一方が導通する。

【０００６】ＦＥＴ１～３がＯＮ，ＦＥＴ４～６がＯＦＦの場合、アンテナＡＮＴからのＲＦ信号は導通状態の第１伝送経路Ａ１を経由して第１処理回路ＲＸ１に流れる。ＦＥＴ４～６はＯＦＦであるため第２伝送経路Ａ２には流れない。このときの各部の電圧について説明する。例えば、ＦＥＴ１～６のピンチオフ電圧ＶＰ＝－０．５Ｖ，順方向電圧ＶＦ＝０．３Ｖとし、制御電圧ＶＣ$_{High}$＝＋２．７Ｖ，ＶＣ$_{Low}$＝０Ｖ（通常、消費電力を節約するためＬｏｗ側は制御電圧を０Ｖとする。）とすると、ＦＥＴ１～３には第１制御電圧ＶＣ１＝＋２．７Ｖ（ＶＣ$_{High}$）が印加されており、ＦＥＴ４～６は第２制御電圧ＶＣ２＝０Ｖ（ＶＣ$_{Low}$）となっている。このとき入力端子ＩＮの電位は、第１制御電圧ＶＣ１と順方向電圧ＶＦとの差で＋２．４Ｖ（ＶＣ$_{High}$－ＶＦ＝２．７Ｖ－０．３Ｖ）となる。この入力端子ＩＮの電位（＋２．４Ｖ）とＦＥＴ１～３またはＦＥＴ４～６の制御電圧ＶＣ１，ＶＣ２との差がゲート電圧ＶＧであり、この場合、ＦＥＴ１～３のゲート電圧ＶＧは＋０．３Ｖ（２．７Ｖ－２．４Ｖ）となりピンチオフ電圧ＶＰである－０．５Ｖよりも大きいためＦＥＴ１～３はＯＮとなる。ＦＥＴ４～６のゲート電圧ＶＧは－２．４Ｖ（０Ｖ－２．４Ｖ）となりピンチオフ電圧ＶＰである－０．５Ｖよりも小さいためＯＦＦとなる。ＯＮ側のＦＥＴ１～３のゲート電流Ｉｇ（図３中に破線矢印で記載）は高電位のＦＥＴ１～３から低電位のＦＥＴ４～６に向かって流れようとするがＦＥＴ４～６はＯＦＦであるため微少なリーク電流しか流れない。また、ＯＮ側のＦＥＴ１～３のゲート電圧ＶＧ（＋０．３Ｖ）とピンチオフ電圧ＶＰ（－０．５Ｖ）の差は０．８ＶでありＲＦ信号による入力端子ＩＮの電位の変動はこの範囲まで許容できる。尚、ＯＦＦ側のＦＥＴ４～６に対しては、この電位の変動は３個のＦＥＴを直列に接続しているため３分の１に低減される。

【０００７】これとは逆に、ＦＥＴ１～３がＯＦＦ，ＦＥＴ４～６がＯＮである場合、ＲＦ信号は導通状態の第２伝送経路Ａ２を経由して第２処理回路ＲＸ２に流れる。ＦＥＴ１～３はＯＦＦであるため第１伝送経路Ａ１にはＲＦ信号は流れない。各部の電圧とＦＥＴ４～６のゲート電流Ｉｇの流れは上記と反対になるだけであるの

で説明を省略する。

【０００８】図４に一例として示すように、ＲＦ信号は交流波形であり入力端子ＩＮの電位を増加または減少させる方向に変動させる。入力端子ＩＮの電位はＯＮ側のＦＥＴのゲート電圧ＶＧを決める一方の電位であるため、これが変動するとゲート電圧ＶＧが変動しピンチオフ電圧ＶＰに対する余裕が増減することになる。すなわち、ＲＦ信号が最大時には入力端子ＩＮの電位とＯＮ側のＦＥＴの制御電圧の差（ゲート電圧ＶＧ）は最少となりピンチオフ電圧ＶＰとの余裕が最も少なくなる。図中には入力端子ＩＮの電位の変動の一部でゲート電圧ＶＧがピンチオフ電圧ＶＰより低くなる場合を示す。

【０００９】

【発明が解決しようとする課題】従来のＩＣスイッチには以下の問題があった。共通な第１端子と第２，第３端子間の接続を、それぞれに直列接続された接合型のＦＥＴのＯＮ／ＯＦＦにより切換えるＩＣスイッチにおいて、ゲート電流Ｉｇが小さいためゲート電圧ＶＧとピンチオフ電圧ＶＰとの差が少なく信号（交流波形）が入力されたとき信号の一部においてＯＮ動作中のＦＥＴをＡＣ的にＯＦＦさせてしまうことがあり挿入損失が生じた。本発明の目的は、信号（交流波形）に対するＯＮ動作中のＦＥＴの動作を安定させ挿入損失が生じることがないようにすることである。

【００１０】一方、特開平１１－４６１０１号公報（先行技術）には図３において入力端子ＩＮに抵抗を介して基準電位を供給し、各ＦＥＴにキャパシタとインダクタの並列共振回路を接続することによって送信時の大入力信号でも出力の歪みを抑えることができるＩＣスイッチが開示されている。しかしながら、先行技術に開示されたＩＣスイッチは有効動作周波数が並列共振回路によって限定されるため、この技術を広い周波数範囲で信号の切換えを行なう図３に示すＩＣスイッチに直ちに適用することは出来なかった。

【００１１】

【課題を解決するための手段】本発明は、上記課題を解決するために提案されたもので、共通の第１端子と第２端子および第３端子の間にそれぞれ接合型のＦＥＴを接続し、各ＦＥＴを交互にＯＮ，ＯＦＦ動作させ第１端子と第２端子および第３端子との間を開閉制御するＩＣスイッチにおいて、第１端子を抵抗を介して接地し、この抵抗の抵抗値を第１端子への信号が最大時にＯＮ動作中のＦＥＴのゲート電位と第１端子の電位との電位差がＦＥＴのピンチオフ電圧より大きくなるように設定したことを特徴とするＩＣスイッチである。

【００１２】

【発明の実施の形態】以下、本発明のＩＣスイッチの一例を図１，２を用いて説明する。図１は１入力２出力型のＩＣスイッチの構成を示す等価回路図であり、図２はＦＥＴのＩＤ－ＶＧ特性の一例とＲＦ信号による入出力端子の電圧の変動との関係を示す説明図である。図３，４と同じ部分には同じ番号を付し説明を省略する。図１に示すＩＣスイッチ１１（図中の一点鎖線で囲んだ部分）は、第１端子としての入力端子ＩＮと第２端子としての第１出力端子ＯＵＴ１間の第１伝送経路Ａ１と、入力端子ＩＮと第３端子としての第２出力端子ＯＵＴ２間の第２伝送経路Ａ２に、それぞれ例えば３個の接合型のＦＥＴ１～３，４～６を直列に接続し、入力端子ＩＮを抵抗Ｒ１を介して接地している。この抵抗Ｒ１は入力端子ＩＮへのＲＦ信号が最大時においてもＯＮ側のＦＥＴの制御電圧と入出力端子の電位との差がピンチオフ電圧ＶＰより大きくなる抵抗値に設定した抵抗Ｒ１である。すなわち、この抵抗Ｒ１を通してゲート電流Ｉｇを増加させ入力端子ＩＮの電位を下げゲート電圧ＶＧとピンチオフ電圧ＶＰとの差を大きくしＦＥＴのＯＮ動作を安定させるように設定する。尚、このとき入力端子ＩＮの電位を下げてもＯＦＦ側のＦＥＴに対しては３個のＦＥＴを直列接続しているため１個のＦＥＴに対してはＯＮ側のＦＥＴの場合に比べて３分の１の電圧変動となり、ピンチオフ電圧ＶＰに対して充分余裕がありＲＦ信号の一部でＯＦＦ側のＦＥＴをＯＮさせることはない。

【００１３】次に、ＩＣスイッチ１１の機能と動作について説明する。ＦＥＴ１～３は第１制御電圧ＶＣ１で、ＦＥＴ４～６は第２制御電圧ＶＣ２でＯＮ／ＯＦＦ制御される。第１制御電圧ＶＣ１と第２制御電圧ＶＣ２とは相補的に印加され、ＦＥＴ１～３がＯＮのときＦＥＴ４～６はＯＦＦとなり、ＦＥＴ１～３がＯＦＦのときＦＥＴ４～６はＯＮとなり第１伝送経路Ａ１または第２伝送経路Ａ２のいずれか一方が導通する。

【００１４】次に、ＲＦ信号の流れをＦＥＴ１～３がＯＮ，ＦＥＴ４～６がＯＦＦの場合について説明する。逆の状態（ＦＥＴ１～３がＯＦＦ，ＦＥＴ４～６がＯＮである場合）についてはＲＦ信号は第２伝送経路Ａ２を流れ、各部の電圧，ＦＥＴ４～６のゲート電流Ｉｇの流れは下記の状態と反対になるだけであるので説明を省略する。アンテナＡＮＴからのＲＦ信号は導通状態の第１伝送経路Ａ１を経由して第１処理回路ＲＸ１に流れる。同時に抵抗Ｒ１側にも若干流れるが抵抗Ｒ１は数十ｋΩであり、ＦＥＴのＯＮ抵抗が数Ωであるため無視できるレベルの損失である。ＦＥＴ４～６はＯＦＦであるため第２伝送経路Ａ２には流れない。このときの各部の電圧について説明する。例えば、ＦＥＴ１～６のピンチオフ電圧ＶＰ＝－０．５Ｖ，順方向電圧ＶＦ＝０．３Ｖとし、制御電圧VC_{High}＝＋２．７Ｖ，VC_{Low}＝０Ｖ（通常、消費電力を節約するためＬｏｗ側は制御電圧を０Ｖとする。）とすると、ＦＥＴ１～３には第１制御電圧ＶＣ１＝＋２．７Ｖ（VC_{High}）が印加されており、ＦＥＴ４～６は第２制御電圧ＶＣ２＝０Ｖ（VC_{Low}）となっている。ゲート電流Ｉｇ（図１中に破線矢印で記載）は高電位のＦＥＴ１～３から低電位のＦＥ

Ｔ４～６及び接地された抵抗Ｒ１を通して流れる。ＦＥＴ４～６はＯＦＦであるため微少なリーク電流しか流れないが抵抗Ｒ１を適切な値に設定することでゲート電流Ｉｇを増加させられ、入力端子ＩＮの電位を所望の電位に下げゲート電圧ＶＧとピンチオフ電圧ＶＰの差をコントロールできる。

【００１５】図２に一例として示すように、ＲＦ信号は交流波形であり入力端子ＩＮの電位を増加または減少させる方向に変動させるが、抵抗Ｒ１を介してゲート電流Ｉｇを流すことで入力端子ＩＮの電位を所望の電位まで下げＯＮ側のＦＥＴの制御電圧との差（ゲート電圧ＶＧ）を大きくしＲＦ信号が最大時においてもピンチオフ電圧ＶＰより大きくするためＯＮ側のＦＥＴをＡＣ的にＯＦＦさせたりすることがない。例えば、接地された抵抗Ｒ１（数十ｋΩ）によりゲート電流Ｉｇを増加させ入力端子ＩＮの電位を＋２．０Ｖに下げるとＯＮ側のＦＥＴのゲート電圧ＶＧは制御電圧＋２．７Ｖ（VC_{High}）と入力端子ＩＮの電位（＋２．０Ｖ）との差（２．７Ｖ－２．０Ｖ＝＋０．７Ｖ）となりピンチオフ電圧ＶＰ（－０．５Ｖ）との電圧差（１．２Ｖ）を大きくできる。これによりＲＦ信号による入力端子ＩＮの電位の変動に対する許容範囲を増加させることができる。このときＯＦＦ側のＦＥＴのゲート電圧ＶＧは制御電圧（VC_{Low}＝０Ｖ）と入力端子ＩＮの電位（＋２．０Ｖ）との差（０Ｖ－２．０Ｖ＝－２．０Ｖ）でピンチオフ電圧ＶＰ（－０．５Ｖ）に対して十分な余裕（１．５Ｖ）を維持できている。

【００１６】尚、上記では第１端子を入力端子とし第２，３端子を出力端子とした１入力２出力型で説明したが、これに限るものではなく各端子はそれぞれ入力，出力，入出力のいずれであってもよい。また、ＦＥＴ１～＊６はｎチャンネル形で説明したがｐチャンネル形であってもよい。ただし、制御電圧のかけ方はｎチャンネル形の場合と反対になる。また、複数のＦＥＴとして３個のＦＥＴを直列接続した場合で説明したがＦＥＴの個数はこれに限るものではなく多いほど耐圧は増加することは言うまでもない。

【００１７】

【発明の効果】以上のように本発明のＩＣスイッチは、共通な第１端子を所定の値に設定した抵抗を介して接地することで第１端子の電位を所望の電位にし信号による第１端子の電位の変動に対してＦＥＴのＯＮ動作を安定させてやることができる。これにより１入力２出力型の移動体通信等に用いられる受信信号を切換えるスイッチＩＣでは、挿入損失の増大を防止できる。接合型のＦＥＴとしては、高速で高周波帯域で動作するガリウムヒ素ＦＥＴがよい。また、ＦＥＴを複数個、直列接続すると、耐電力性がアップするとともに信号による電位の変動はＯＦＦ状態の直列接続されたＦＥＴの個数で除した値になり、ＯＦＦ状態のＦＥＴのゲート電圧ＶＧとピンチオフ電圧ＶＰの差を大きくしＯＦＦ動作を安定させてやることができる。

【図面の簡単な説明】

【図１】本発明のＩＣスイッチの構成を示す等価回路図

【図２】本発明のＩＣスイッチを構成するＦＥＴのＩＤ－ＶＧ特性の説明図

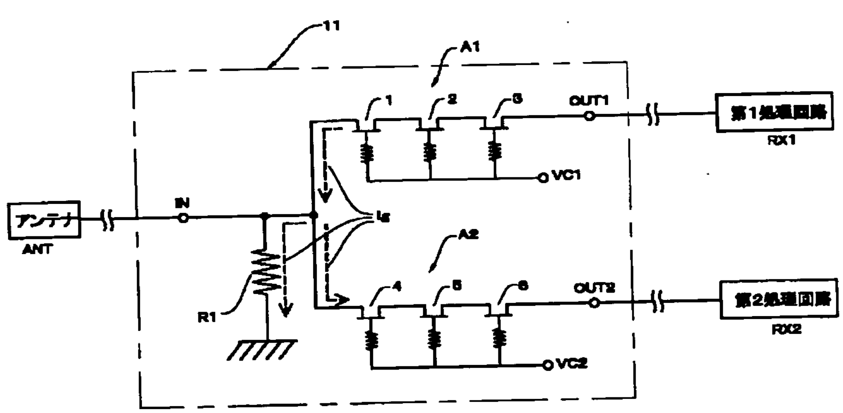
【図３】従来のＩＣスイッチの構成を示す等価回路図

【図４】従来のＩＣスイッチを構成するＦＥＴのＩＤ－ＶＧ特性の説明図

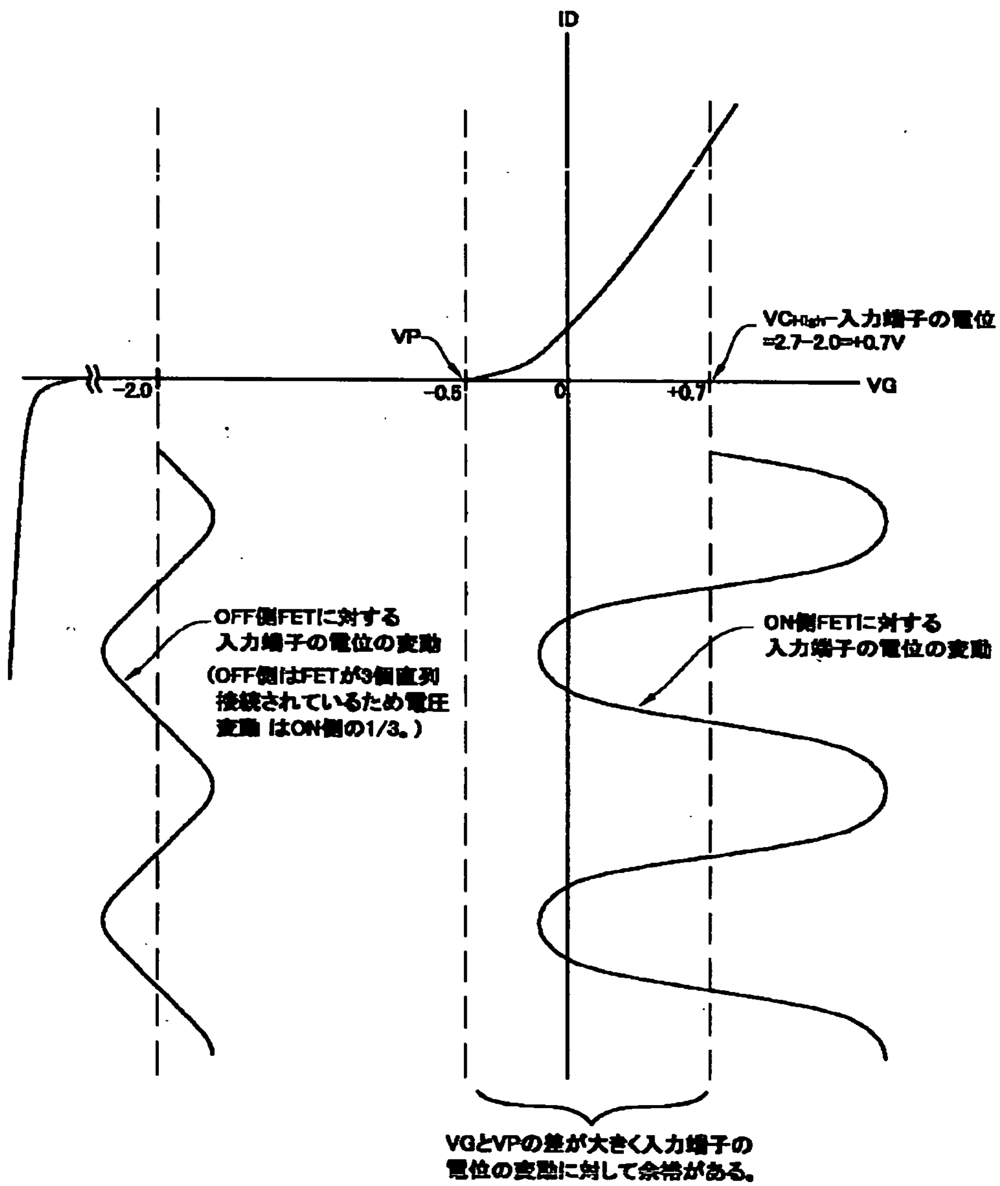
【符号の説明】

Ｒ１　抵抗

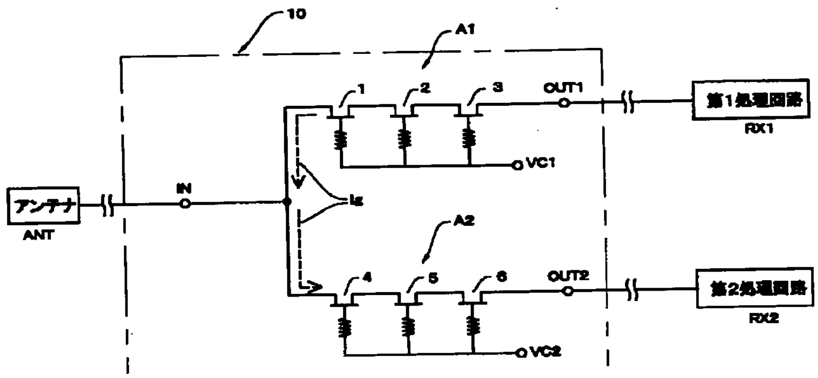
【図１】



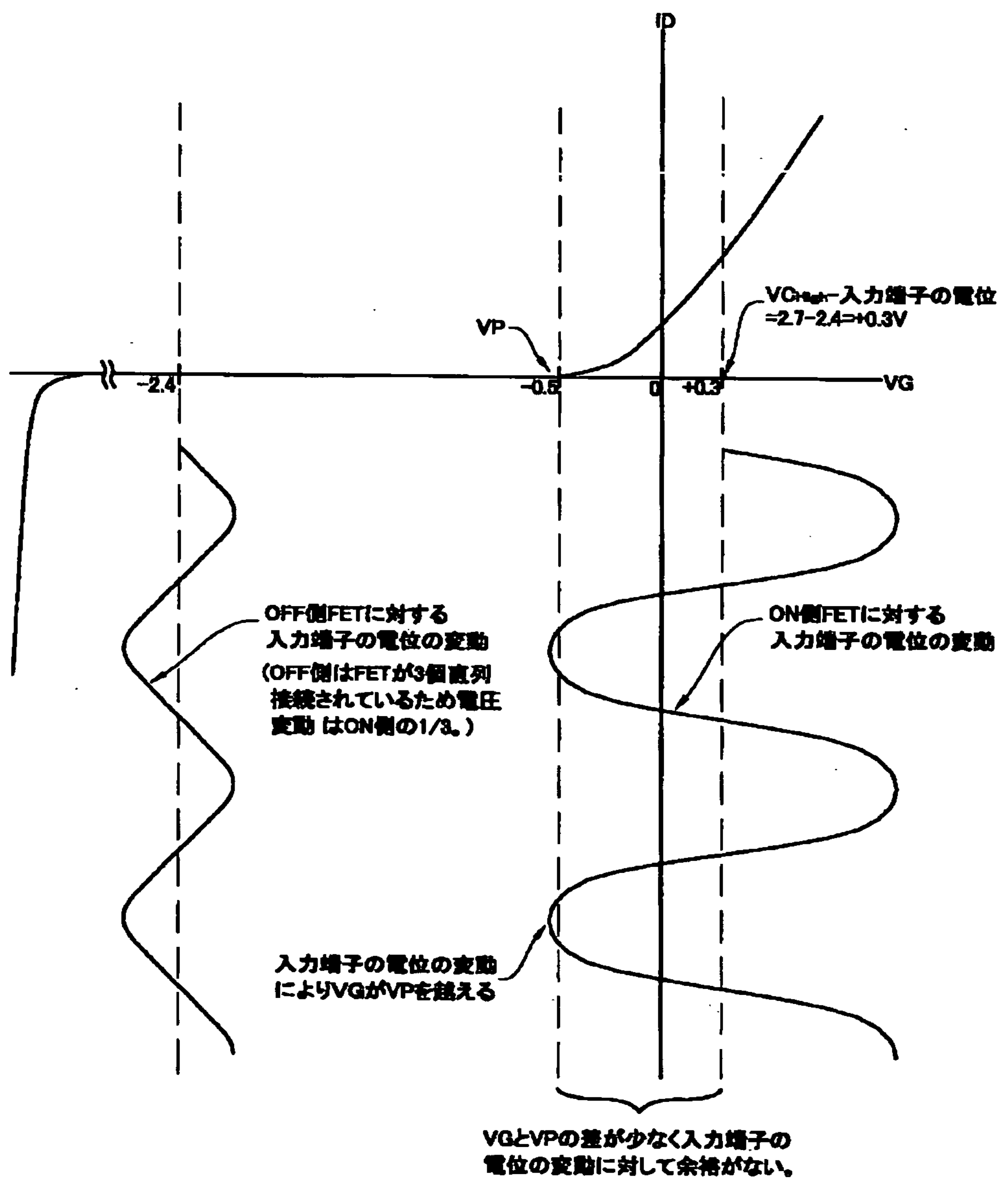
【図２】


ID
VP
VCHigh−入力端子の電位
=2.7−2.0=+0.7V
−2.0
−0.5
0
+0.7
VG
OFF側FETに対する
入力端子の電位の変動
(OFF側はFETが3個直列
接続されているため電圧
変動 はON側の1/3。)
ON側FETに対する
入力端子の電位の変動
VGとVPの差が大きく入力端子の
電位の変動に対して余裕がある。

【図３】


10
A1
1
2
3
OUT1
第1処理回路
RX1
VC1
アンテナ
ANT
IN
Ig
A2
4
5
6
OUT2
第2処理回路
RX2
VC2

【図４】


ID
VG
VP
VCHigh−入力端子の電位
=2.7−2.4=+0.3V
−2.4
−0.5
0
+0.3
OFF側FETに対する
入力端子の電位の変動
(OFF側はFETが3個直列
接続されているため電圧
変動はON側の1/3。)
ON側FETに対する
入力端子の電位の変動
入力端子の電位の変動
によりVGがVPを越える
VGとVPの差が少なく入力端子の
電位の変動に対して余裕がない。

Original document

IC SWITCH

Patent number: JP2002135095
Publication date: 2002-05-10
Inventor: HAMASE SEIJI
Applicant: KANSAI NIPPON ELECTRIC
Classification:
- international: H03K17/00; H01P1/15; H03K17/693
- european:
Application number: JP20000326674 20001026
Priority number(s): JP20000326674 20001026

Also published as:
US200205144

View INPADOC patent family

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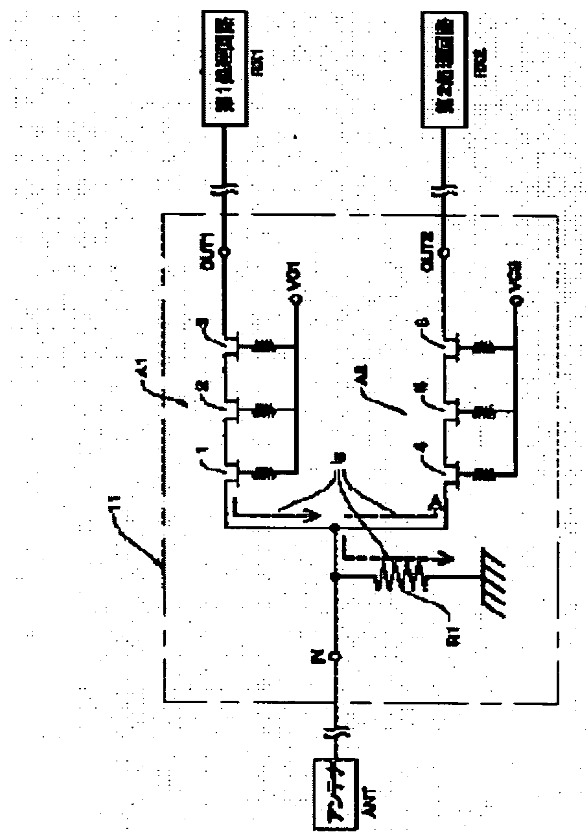
Abstract of **JP2002135095**

PROBLEM TO BE SOLVED: To solve the problem of generation of an insertion loss in a conventional IC switch for switching connection between a common 1st terminal and a 2nd terminal or a 3rd terminal by the on/off of junction type FETs connected to respective terminals in series because a gate current Ig is small, the difference between a gate voltage VG and a pinch off voltage VP is reduced, and an FET in on-operation may be turned off like an AC frequency when a signal (of an AC waveform) is inputted. SOLUTION: In the IC switch 11, three junction type FETs 1 to 3, and 4 to 6, respectively, e.g. are connected in series to a 1st transmission route A1 between an input terminal IN and 1st output terminal OUT1 and to a 2nd transmission route A2 between the input terminal IN and a 2nd output terminal OUT2, and the input terminal IN is grounded through a resistor R1. The resistor R1 is set up to a resistance value capable of increasing a potential difference between the control voltage VCHigh of the on-side FET and the input terminal IN to a level larger than the pinch off voltage VP when a signal inputted to the input terminal IN is maximum.



Description of corresponding document: **US2002051444**

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a switch circuit.

[0003] 2. Description of the Related Art

[0004] Each transceiver employed in mobile communications includes a switch circuit for switching an input path from an output path of high-frequency signals.

[0005] The switch circuit includes FETs (Field Effect Transistors) in the input and output paths, to open or close the patl respectively The switch circuit activates either FETs arranged in the input path or FETs arranged in the output path, and inactivates the other one FET, thereby to switch the path from one to another through which high-frequency signals flow

[0006] In the case where a large amplitude signal is input to the above switch circuit the FETs may undesirably be opera as to deteriorate the waveform of their output signals.

[0007] In a switch circuit disclosed in Unexamined Japanese Patent Application KOKAI Publication Ser. No. H11-4610 prevent the deterioration in the waveform of output signals when a large amplitude signal is input to the switch circuit, a inductor and a capacitor are connected in parallel with each other between the source and drain of each FET.

[0008] However, the frequency of input signals, which can be effected by the structure including the inductor and capaci being connected with each other, is limited by a resonance circuit including an inductor and a capacitor. In other words, signal has the frequency which is not in a frequency range to be limited by the resonance circuit, the waveform of output may be deteriorated. Hence, a problem is that the technique disclosed in Unexamined Japanese Patent Application KOK Publication Ser. No. H11-46101 can not be adapted for those switch circuits handling signals in a wide range of frequen

[0009] The entire contents of Unexamined Japanese Patent Application KOKAI Publication Ser. No. H11-46101 are incorporated herein by reference.

SUMMARY OF THE INVENTION

[0010] The present invention has been made in consideration of the above. It is accordingly an object of the present inve provide a switch circuit which operates stably regardless of the signal frequency.

[0011] In order to achieve the above object, according to the first aspect of the present invention, there is provided a swi circuit comprising;

[0012] a first transistor which is connected between a first terminal and a second terminal,

[0013] a second transistor which is connected between the first terminal and a third terminal; and

[0014] a resistor one end of which is connected to the first terminal and other end of which is grounded, and

[0015] wherein either the first transistor or the second transistor is controlled to be ON, and

[0016] the resistor has a resistance value which is set at such a value that a difference between a gate voltage of the first transistor or second transistor being ON and a pinch-off voltage of the first transistor or second transistor being ON is se than an amplitude of a potential of the first terminal which varies by a signal flowing to the first terminal.

[0017] According to this invention, there can he provided a switch circuit is stably operated regardless of the frequency signal flowing to the first terminal.

[0018] In the switch circuit;

[0019] the first transistor may include a plurality of transistors which are connected with each other in series between the terminal and the second terminal; and

[0020] the second transistor include a plurality of transistors which are connected with each other in series between the f terminal and the third terminal.

[0021] In the switch circuit,

[0022] each of the first transistor and the second transistor may be a junction-type Field Effect Transistor which is forme gallium arsenic.

[0023] In the switch circuit:

[0024] the resistor may be a variable resistor; and

[0025] the switch circuit may further include

[0026] a measurement circuit which measures the amplitude of the potential of the first terminal, and

[0027] a control circuit which sets a resistance value of the resistor in accordance with the amplitude measured by the measurement circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] The object and other objects and advantages of the present invention will become more apparent upon reading of following detailed description and the accompanying drawings in which:

[0029] FIG. 1 is a diagram showing an equivalent circuit of an IC switch according to an embodiment of the present inv

[0030] FIG. 2 is a diagram showing the relationship between the ID-VG characteristics of an FET included in the IC swi FIG. 1 and the potential variation of an input terminal upon reception of an RF signal, in the case where the resistance v resistor included in the IC switch of FIG. 1 is infinite;

[0031] FIG. 3 is a diagram showing the relationship between the ID-VG characteristics of the FET included in the IC sw FIG. 1 and the potential variation of the input terminal upon reception of an RF signal, in the case where the resistance v the resistor included in the IC switch of FIG. 1 is several ten k[Omega]; and

[0032] FIG. 4 is a diagram showing another structure of the IC switch according to the embodiment of the present inven

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0033] An IC switch according to an embodiment of the present invention will now be depicted with reference to the accompanying drawings.

[0034] FIG. 1 shows an equivalent circuit of an IC switch 11 according to this embodiment.

[0035] The IC switch 11 includes a resistor R1 and a plurality of FETs (Field Effect Transistors). In FIG. 1, the IC switc includes six FETs 1 to 6, for example. Each of the FETs 1 to 6 is an n-channel junction-type FET which is formed of gal arsenic.

[0036] The IC switch 11 has an input terminal IN, the first output terminal OUT1, the second output terminal OUT2, the control terminal VC1 and the second control terminal VC2.

[0037] The FETs 1, 2 and 3 are connected in series along the first path A1 between the input terminal IN and the first ou terminal OUT1. The gate of each of the FETs 1, 2 and 3 is connected to the first control terminal VC1. The FETs 1, 2 an operate in accordance with a control voltage supplied from a control circuit CR connected to the first control terminal V

[0038] The FETs 4, 5 and 6 are connected in series along the second path A2 between the input terminal IN and the seco output terminal OUT2. The gate of each of the FETs 4, 5 and 6 is connected to the second control terminal VC2. The FE and 6 operate in accordance with a control voltage supplied from a control circuit CR connected to the second control te VC2.

[0039] The control voltage to be applied to the gate of each of the FETs 1, 2 and 3 and the control voltage to be applied t FETs 4, 5 and 6 are complementary to each other. Specifically, in the case where the control voltage to be applied to eac FETs 1, 2 and 3 is at a high level, the control voltage to be applied to each of the FETs 4, 5 and 6 is at a low level. On th in the case where the control voltage to be applied to each of the FETs 1, 2 and 3 is at a low level, the control voltage to applied to each of the FETs 4, 5 and 6 is at a high level. In this structure, then, either one of the first path A1 and the sec A2 is in a conductive state.

[0040] An antenna ANT is connected to the input terminal IN, and the first processing circuit RX1 is connected to the fi output terminal OUT1, and the second processing circuit RX2 is connected to the second output terminal OUT2.

[0041] RF (Radio Frequency) signals are transmitted between the antenna ANT and the first processing circuit RX1 or b the antenna ANT and the second processing circuit RX2, respectively through the first path A1 or the second path A2.

[0042] The first processing circuit RX1 executes a predetermined signal process for RF signals (high-frequency signals) supplied from the antenna ANT. Otherwise, the first processing circuit RX1 sends RF signals for which a predetermined process is done, to the antenna ANT.

[0043] The second processing circuit RX2 executes a predetermined signal process for RF signals supplied from the ant ANT. Otherwise, the second processing circuit RX2 sends RF signals for which a predetermined signal process is done, antenna ANT.

[0044] One end of the resistor R1 is connected to the input terminal IN, and the other end thereof is grounded. The resist value of the resistor R1 is set at such a value that a difference between the gate voltage VG of the FET and the pinch-off thereof is larger than the amplitude of the RF signals, as will more specifically be explained later. In this structure, those 2 and 3 or FETs 4, 5 and 6 which are ON will not be OFF upon reception of an RF signal.

[0045] Functions and operations of the IC switch 11 according to the embodiment of the present invention will now be described.

[0046] Explanations will now be made to the IC switch 11, particularly in the case where the FETs 1, 2 and 3 are ON an FETs 4, 5 and 6 are OFF. Now, let it be assumed that the potential (VCHigh) of the first control terminal VC1 is +2.7V, potential (VCLow) of the second control terminal VC2 is 0V, the forward voltage VF of each of the FETs 1, 2 and 3 is + and the pinch-off voltage VP of each of the FETs 1 to 6 is -0.5V.

[0047] In the case where the resistance value of the resistor R1 is infinite, the potential of the input terminal IN is +2.4V is obtained by subtracting the forward voltage VF (=+0.3V) from the potential (VCHigh=+2.7V) of the first control term VC1. In other words, the gate voltage VG of each of the FETs 1, 2 and 3 is +0.3V which is obtained by subtracting the p (+2.4V) or the input terminal IN from the potential (VCHigh=+2.7V) of the first control terminal VC1. In this manner, t voltage (=+0.3V) of each of the FETs 1, 2 and 3 is greater than the pinch-off voltage VP (=-0.5V), resulting in that the F and 3 are ON.

[0048] In the case where the resistance value of the resistor R1 is infinite, the gate voltage VG of each of the FETs 4, 5 a 2.4V which is obtained by subtracting the potential (+2.4V) of the input terminal IN from the potential (VCLow=0V) of second control terminal VC2. In this manner, the gate voltage (=-2.4V) of each of the FETs 4, 5 and 6 is smaller than the off voltage VP (-0.5V), resulting in that the FETs 4, 5 and 6 are OFF.

[0049] In the above circumstances, if an RF signal flows to the input terminal IN, the potential of the input terminal IN v an amount corresponding to the amplitude of the RF signal as shown in FIG. 2. Upon this, the gate voltage VG of each o FETs 1, 2 and 3 varies by an amount corresponding to the amplitude of the RF signal. For example, in the case where th amplitude of the RF signal is +1.0V, the potential of the input terminal IN varies in a range from +1.4V to +3.4V, and th voltage VG of each of the FETs 1, 2 and 3 varies in a range from -0.7V to -1.3V. In this case, as illustrated in FIG. 2A, t voltage VG of each of the FETs 1, 2 and 3 may be lower than their pinch-off voltage VP. Hence, any of those FETs 1, 2 which is ON may periodically be OFF.

[0050] Because the FETs 4, 5 and 6 are connected with each other in series, the effect of the potential variation is divide three, so that one third of the effect is delivered to each of the FETs 4, 5 and 6. In other words, the variation of the gate v VG of each of the FETs 4, 5 and 6 is one third the variation of the gate voltage VG of each of the FETs 1, 2 and 3. Thus, those FETs 4, 5 and 6 which is OFF will not be ON upon reception of the RF signal.

[0051] If the resistance value of the resistor R1 is set at such a value that a difference between the gate voltage VG of ea FETs 1, 2 and 3 and its pinch-off voltage VP is greater than the amplitude of the RF signal, i.e. the amplitude of potentia input terminal IN which varies upon reception of the RF signal, the above-described potential variation of the input term can be prevented from having an effect on the FETs 4, 5 and 6,

[0052] Gate current IG flows in a direction from high-potential points to low-potential points. Specifically, in this case, t current IG flows from the FETs 1, 2 and 3 to the FETs 4, 5 and 6 and the resistor R1 (in the directions denoted by broke shown in FIG. 1).

[0053] The gate current IG flowing to the FETs 4, 5 and 6 is very little, because the FETs 4, 5 and 6 are OFF.
[0054] The amount of gate current IG flowing to the resistor R1 may vary depending on the resistance value of the resist Hence, if the resistance value of the resistor R1 is adjusted, the potential of the input terminal IN can be adjusted. Specif the lower the resistance value becomes, the gate current IG, flowing to the resistor R1 gets greater and the potential of th terminal IN gets lower.
[0055] In the case where the resistance value of the resistor R1 is set at several ten k[Omega], e.g. within a range from 3 k[Omega], the potential of the input terminal IN will approximately be +2.0V. In the case where the potential of the inpu terminal IN is set at +2.0V, the gate voltage VG of each of the FETs 1, 2 and 3 is +0.7V. Hence, the difference between voltage VG and pinch-off voltage VP is +1.2V. This difference is greater than the amplitude (+1.0V) of the RF signal, a in FIG. 3. Thus, the FETs 1, 2 and 3 will not be OFF by the effect of the potential variation of the input terminal IN.
[0056] In the case where the resistance value of the resistor R1 is several ten k[Omega], the gate voltage VG of each of t 4, 5 and 6 is -2.0V which can be obtained by subtracting the potential (+2.0V) of the input terminal IN from the potentia (VCLow=0V) of the second control terminal VC2. Since the gate voltage VG (-2.0V) is smaller than the pinch-off volta 0.5V), each of the FETs 4, 5 and 6 will be OFF.
[0057] In this case as well, as shown in FIG. 3, the effect of the potential variation of the input terminal IN is divided int so that only one third of the effect is delivered to each of the FETs 4, 5 and 6. The variation of the gate voltage VG of ea the FETs 4, 5 and 6 is one third of the variation of the gate voltage VG of each of the FETs 1, 2 and 3. Thus, each of the 5 and 6 which is being OFF will not be ON upon reception of the RF signal.
[0058] If the resistance value of the resistor R1 is set at a value which is sufficiently larger than the resistance value (sev [Omega]) of each of the activated FETs 1, 2 and 3, i.e. at several ten k[Omega], only a very small amount of RF signal c to the resistor R1, and hence resulting in only negligible loss of RF signal.
[0059] The functions and operations of the IC switch 11 in the case where the FETs 1, 2 and 3 are OFF and the FETs 4, are ON are substantially the same as the above, except that the FETs 1, 2 and 3 are switched to the FETs 4, 5 and 6.
[0060] As explained above, the input terminal IN is grounded through the resistor R1, and the resistance value of the res is adjusted, thereby stably operating the IC switch 11. Since the operations of the IC switch 11 is stably operated by the R1, the switch circuit 11 can stably process signals in a wide range of frequency band
[0061] As illustrated in FIG. 4, the IC switch 11 may include a variable resistor R2 in place of the resistor R1, and may f has a measurement circuit 7 and a control circuit 8. The measurement circuit 7 measures the variation width of the poten the input terminal IN or the amplitude of the RF signals flowing to the input terminal IN. The control circuit 8 includes a decoder, etc., and sets the resistance value of the variable resistor R2 in accordance with the variation width of the poten amplitude measured by the measurement circuit 7. In this structure, the resistance value of the variable resistor R2 can b changed in accordance with the variable width of the potential of the input terminal IN or the amplitude of the RF signal hence realizing the IC switch 11 which can stable be operated even upon reception of R1 signals with various amplitude
[0062] Each of the FETs 1 to 6 may be a p-channel FET instead of an n-channel FET. It is preferred that each of the FE be formed of gallium arsenic so as to operate in a high frequency band at a high rate.
[0063] The number of the FETs is not limited to six. The more the number of the FETs being connected with each other becomes, the less the potential variation of the input terminal IN has an effect on the FETs being OFF. Thus, the more th number of FETs being connected with each other in series, the more the IC switch11 becomes stably operable.
[0064] Various embodiments and changes may be made thereonto without departing from the broad spirit and scope of t invention. The above-described embodiment is intended to illustrate the present invention, not to limit the scope of the p invention. The scope of the present invention is shown by the attached claims rather than the embodiment. Various modifications made within the meaning of an equivalent of the claims of the invention and within the claims are to be re to be in the scope of the present invention.
[0065] This application is based on Japanese Patent Application Ser. No. 2000-326674 filed on Oct. 26, 2000, and inclu specification, claims, drawings and summary. The disclosure of the above Japanese Patent Application is incorporated h reference in its entirety.

Claims of corresponding document: **US2002051444**

What is claimed is:

1. A switch circuit comprising;
a first transistor which is connected between a first terminal and a second terminal;
a second transistor which is connected between said first terminal and a third terminal; and
a resistor one end of which is connected to said first terminal and other end of which is grounded, and
wherein either said first transistor or said second transistor is controlled to be ON, and
said resistor has a resistance value which is set at such a value that a difference between a gate voltage of said first transi second transistor being ON and a pinch-off voltage of the first transistor or second transistor being ON is set greater thar amplitude of a potential of said first terminal which varies by a signal flowing to said first terminal.

2. The switch circuit according to claim 1, wherein:
said first transistor includes a plurality of transistors which is connected with each other in series between said first term

said second terminal; and
said second transistor includes a plurality of transistors which is connected with each other in series between said first te
and said third terminal.

3. The switch circuit according to claim 2, wherein each of said first transistor and said second transistor is a junction-ty
Effect Transistor which is formed or gallium arsenic.

4. The switch circuit according to claim 1, wherein:
said resistor is a variable resistor; and
said switch circuit further includes
a measurement circuit which measures the amplitude of the potential of said first terminal, and
a control circuit which sets a resistance value of said resistor in accordance with the amplitude measured by said measur
circuit.
